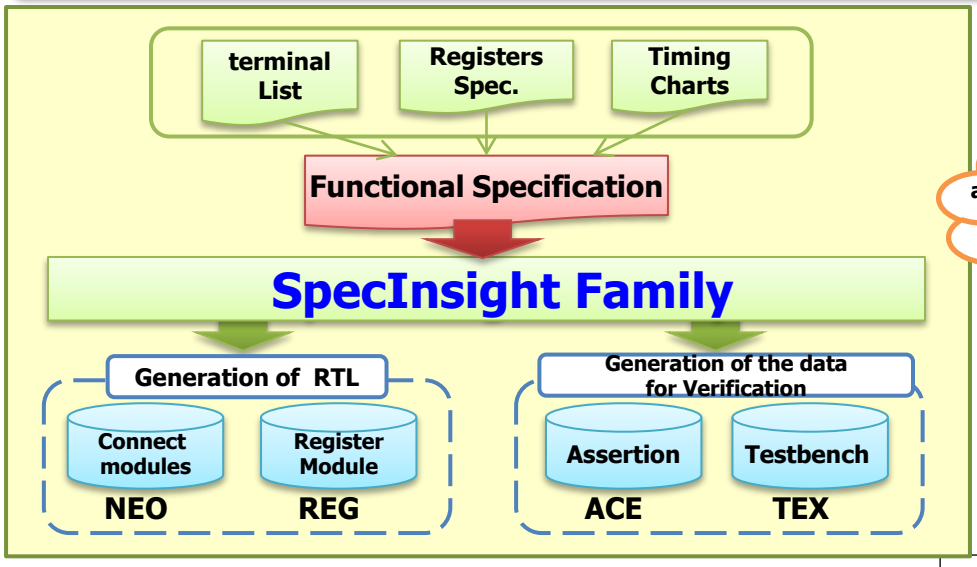
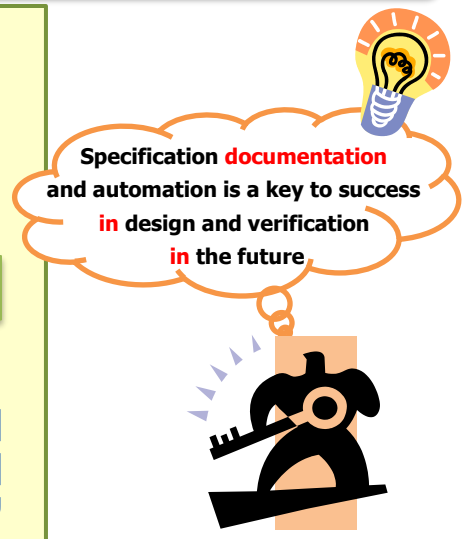
SpecInsight

Tool for automatically generating the RTL and verification data from input specification





SpecInsight-NEO(Connect modules)

[Function]
- Generate the inter-module connection RTL from signals table and connection information.
- Select Verilog or VHDL for RTL coding.

[Feature]
- Create Signals table, connection information in Excel. Also be used as your format.
- Check the mismatch of input and output definition and bit width.

[Advantage]
- Be released after creating connection without mistake.

AXIバス20	A0_WID	I	clk	–	8		
	A0_WDATA	I	clk	–	64		
	A0_WLAST	I	clk	P	1		
	A0_WSTRB	I	clk	–	8		
	A0_WREADY	O	clk	P	1	1'b0	
	A0_BID	I	clk	–	8		
	A0_BRESP	I	clk	–	2		
	A0_BVALID	I	clk	–	1		
	A0_BREADY	O	clk	P	1	1'b0	
	A0_ARID	I	clk	–	8		
	A0_ARADDR	I	clk	–	32		
	A0_ARLEN	I	clk	–	5		
	A0_ARSIZE	I	clk	–	3		

Fig.1 Example of Signals Table

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity a1 is
port (
  clk      : in   std_logic; -- Clock
  rst_x    : in   std_logic; -- hardware set
  A1_AWID    : in   std_logic_vector( 7 downto 0 );
  A1_AWADDR  : in   std_logic_vector( 31 downto 0 );
  A1_AWLEN   : in   std_logic_vector( 4 downto 0 );
  A1_AWSIZE  : in   std_logic_vector( 2 downto 0 );
  A1_AWBURST : in   std_logic_vector( 2 downto 0 );
  A1_AWLOCK  : in   std_logic;
    ・・・
```

Fig.2 Example of RTL Output

SpecInsight-REG(Generation of Registers module)

[Function]
- Generate a register module RTL from the register spec.
- Select Verilog or VHDL for RTL coding.
- Support the standard bus interface.

[Feature]
- Check the mistake of duplication of address map and the register name.
- Support AXI, AHB, APB.

[Advantage]
- Although there are many register, it can generate RTL easily if the register specifications are defined.
- Unify the format of specifications and RTL

BaseAddress Group Block	Size (Byte)	Group Name Block Name Field Name	Bit Assign	Bus Access Property	Reset Initial value Async	Connection Output Internal I/F	Remark Note1 Description
0x000		MAC					
0x04		INT_SOURCE					Interrupt Source Register
		TXB	[0]	RW	0	Iv,O	Transmit Buffer
		TXE	[1]	RW	0	Iv,O	Transmit Error
		RXF	[2]	RW	0	Iv,O	Receive Frame
		RXE	[3]	RW	0	Iv,O	Receive Error
		BUSY	[4]	RW	0	Iv,O	Busy
		TXC	[5]	RW	0	Iv,O	Transmit Control Frame
		RXC	[6]	RW	0	Iv,O	Receive Control Frame
		yoyaku	[31:7]	RSVD	0	None	
0x08		INT_MASK					Interrupt Mask Register
		TXB_M	[0]	RW	0	O	Transmit Buffer Mask
		TXE_M	[1]	RW	0	O	Transmit Error Mask
		RXF_M	[2]	RW	0	O	Receive Frame Mask
		RXE_M	[3]	RW	0	O	Receive Error Mask

Fig.3 Example of Registers Specification

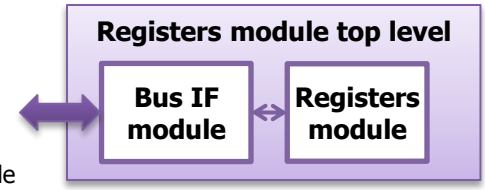


Fig.4
Configuration of
The Registers module

SpecInsight-ACE(Generation of Assertion code)

[Function]
- ・Create a timing chart in a dedicated editor.
- ・Define the assertion specification on the timing chart.
- ・Generate the System Verilog Assertion from assertion specification.

[Feature]
- ・Create a timing chart easily.
- ・Define an assertion without knowing the assertion language.
- ・Output an assertion description that was defined in Figure.

[Advantage]
- ・Adopt the assertion-based verification easily.
  ※ Detailed knowledge on the assertion is not required.
- ・Be easier to review for contents can be displayed in the figure
- ・Reuse assertion and Timing chart easily.

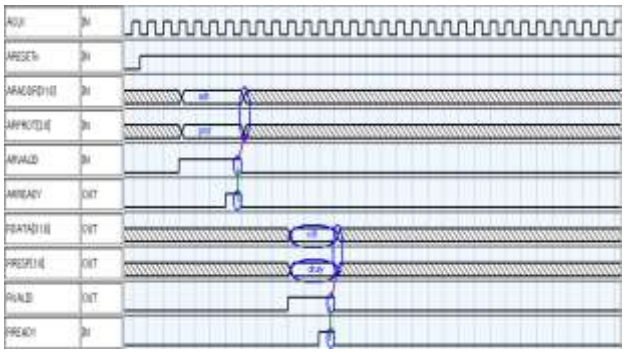


Fig.5 Example of Timing Chart (For Specification)

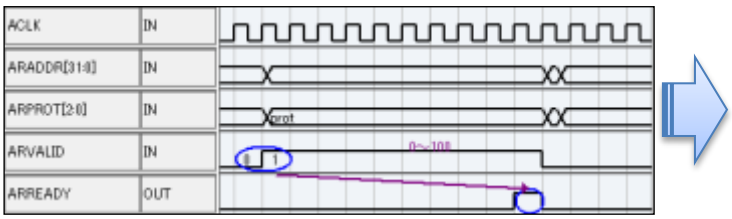


Fig.6 Example of assertion definition

Fig.7 Example of Assertion Code Output

[Product page] Please see the FAQ and videos http://cmengineering.co.jp/products/specinsight-ace.html

SpecInsight-TEX (Generation of Testbench code)

[Function]
- ・Generate the input data of the Testbench from the timing chart basing specification.
- ・Create a verification scenario by combining a plurality of timing charts.
- ・Choose Verilog or VHDL for Testbench

[Feature]
- ・Create a Testbench with a simple operation.
- ・Auto connect RTL and Testbench from Signals table.
- ・Import assertion which is generated in SpecInsight-ACE easily .

[Advantage]
- ・Run a simulation easily even for the inexperienced person in Testbench.
- ・Check the operation by simulation early in design.

Fig.8 Example of test bench Output

[Product page] Please see the FAQs and videos http://cmengineering.co.jp/products/specinsight-tex.html

Item	Support Platform	Remarks
OS	Windows8/7	
Microsoft Office	Excel2013/2010/2007	
Simulator	VCS/IES/ModelSim(※)	※Assertion: ModelSim DE
FPGA Tool	Xilinx:ISE, Altera:Quartus II	SpecInsight-NEO

* Products are subject to change without prior notice.

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